A chalcogenide-based device with potential for multi-state storage

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Abstract

We have investigated electrical properties of a chalcogenide-based device with naturally oxidized Al electrodes. Intermediate-resistance (IR) states exhibited by current–voltage (I–V) characteristics, dynamic resistance change as a function of pulse height and decay behavior from a low-resistance state of such a device make multi-state storage feasible. These IR states could be induced by electrical pulses and stable in a period. Device resistances of such a series of states might be related to the number of dendrite filaments across the chalcogenide channel.
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1. Introduction

Phase change materials mainly include two families, namely nucleation-dominated chalcogenide alloys domination in terms of time-limited factors [1] and growth-dominated chalcogenide alloys. The former alloys are the pseudo-binary $(GeTe)_x(Sb_2Te_3)_y$ alloys in which the crystallization is controlled by nucleation of crystals, while the latter alloys are Ag- and In-doped Sb_2Te alloys in which crystallization occurs by motion of a glass–crystal interface [1,2].

Currently, phase change memory (PCM) is thought of as a favorite candidate for next-generation non-volatile memories [3–7]. PCM technology is simply based upon resistance change due to the reversible structural transformation of chalcogenides between disordered amorphous (high resistivity) and ordered crystalline (low resistivity) phases [8,9]. Most of reported PCM devices have a vertical structure composed of a chalcogenide layer of GeSbTe alloys sandwiched by a bottom resistive electrode of refractory metal nitrides and a top metal electrode [4,5,10–12].

Today most of research on PCM devices is focused on binary storage. To our knowledge, there are very few reports on multi-state storage of PCM devices, which is on the basis of changeable amorphous volume fraction induced by a series of electrical pulses [3]. In addition, particularly, there is no detailed information on it.

In this paper, we adopted a lateral structure composed of a chalcogenide channel connected by naturally oxidized Al electrodes. After initially annealing and breakdown, characteristics of these devices showed that there existed some intermediate-resistance (IR) states between low-resistance (LR) and high-resistance (HR) states. They were very promising for multi-state storage application.

2. Experimental method

Fig. 1 shows an optical microscope image and schematic diagram of our 16 fabricated devices. SiO_2 was first thermally grown on the Si substrate, and this was followed by Al electrode deposition. The gap between two Al source (S) and drain (D) electrodes is 3 μm and the width of each Al electrode is 30 μm. Al electrodes were then naturally oxidized in air. A layer of 20-nm-thick $Ge_2Sb_2Te_5$ (GST) or 40-nm-thick AgInSbTe (AIST) chalcogenide was then sputtered. A capping layer of ZnS–SiO_2 was finally

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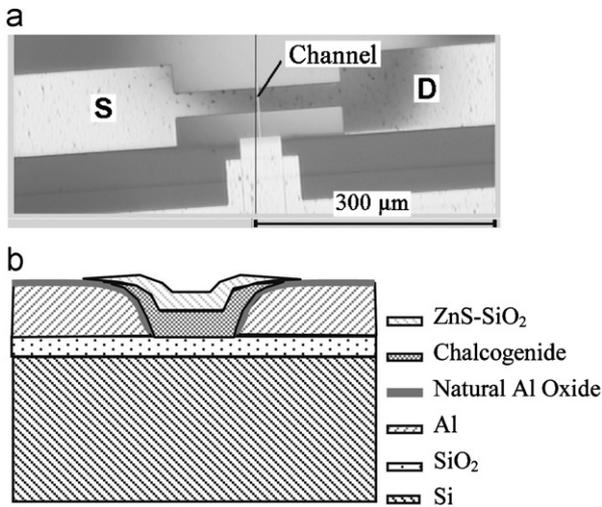
Fig. 1. (a) An optical microscope image and (b) schematic diagram of the chalcogenide-based device with naturally oxidized Al electrodes.

Fig. 2. I–V characteristics of a device exhibiting two intermediate-resistance (IR) states.

Fig. 3. Device resistance as a function of pulse height of: (a) LR-to-HR RESET and (b) HR-to-LR SET operations via IR states.

sputtered onto the chalcogenide material to protect it from oxidation as well as mechanical damage. We annealed device samples at approximately 200 °C to crystallize the chalcogenide channel [6,7] and performed breakdown of natural oxide on electrodes at a relatively high voltage before electrical measurement was started. Current–voltage (I–V) characteristics of device samples were measured using a semiconductor parameter analyzer (4155B, Agilent Technologies) in air at room temperature. Single voltage pulses with a width of 90 ms generated by the semiconductor parameter analyzer were adopted in the measurements.

3. Results and discussion

3.1. I–V characteristics exhibiting IR states

The I–V characteristics of these devices by sweeping from a negative bias voltage to a positive bias voltage and backward are typically shown in Fig. 2. In the forward sweeping direction, an LR (or SET) state remained at first at the negative polarity, while it could be switched to an HR (or RESET) state at an LR-to-HR switching point. Here we call the voltage at the switching point the LR-to-HR threshold voltage V_{thl-h}. The LR-to-HR threshold voltage varies from approximately 4 to 15 V from sample to sample. Let us take a close look at the switching from the LR to HR state. It is clearly seen that there exist two IR states in the LR-to-HR switching as indicated in the figure. After we swept the bias in the backward direction, the former induced HR state remained, except that the bias reached a certain voltage at an HR-to-LR switching point, which is called the HR-to-LR threshold voltage V_{thh-l}.

I–V characteristics of the devices hence show asymmetry with respect to the polarity of bias. The LR state can be switched to another HR state at voltages higher than a certain bias voltage, while the resulting HR state can only be reversed to the former LR state at voltages lower than a
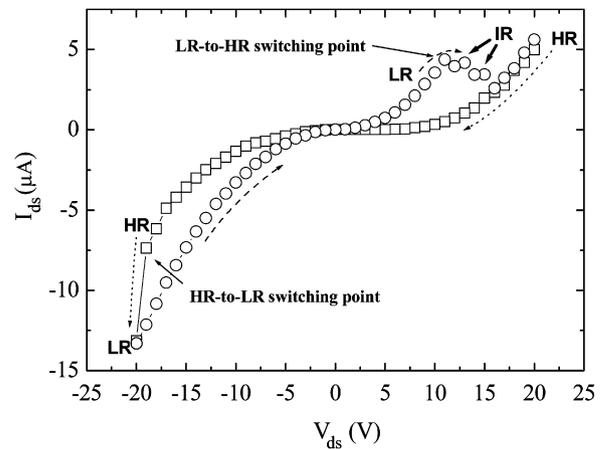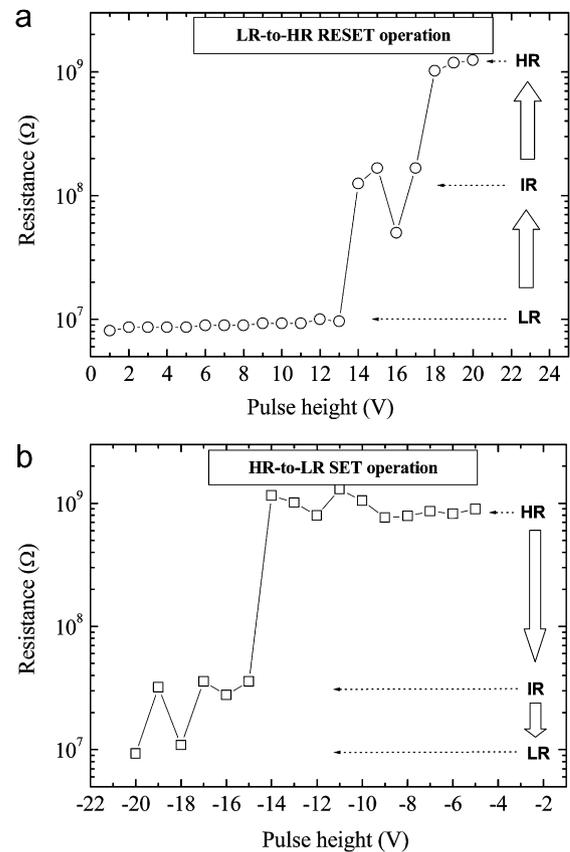
certain bias voltage at the opposite polarity. Here we refer to the phenomenon as the bias polarity-dependent switching.

3.2. Reversible switching in electrical pulse mode

Experiments for LR-to-HR RESET and HR-to-LR SET operations were done at first. Fig. 3(a) shows the typical experimental results for LR-to-HR RESET operation.

The measurement began with an LR state of approximately $8 \times 10^6 \, \Omega$. Pulses with increasing pulse heights from $+1$ to $+20 \, V$ were applied to the device. Resistance was read at a low voltage after each pulse application. Device resistance does not change at relatively low pulse height. However, the resistance was markedly increased by approximately one order of magnitude to approximately $1 \times 10^8 \, \Omega$ after a pulse of $+14 \, V$ was applied. This IR state was relatively stable from $+14$ to $+17 \, V$. By further increase of pulse height, the device resistance increased from the IR state to a HR state of $1 \times 10^9 \, \Omega$ at $+18 \, V$.

Fig. 3(b) shows the typical experimental results for HR-to-LR SET operation. The measurement began with the HR state immediately after the above experiment of LR-to-HR RESET operation. Pulses with heights from -5 to $-20 \, V$ with an interval of $1 \, V$ were applied to the above device. Resistance was also read after each of pulse application. Device resistance dropped to an IR state of approximately $3.5 \times 10^7 \, \Omega$ at $-15 \, V$ and it further decreased to the LR state of approximately $8 \times 10^6 \, \Omega$ at $-20 \, V$.

It could be clearly seen from the relationship between device resistance and pulse height that there also existed some IR states for the device reported here, and these IR states were relatively stable in a certain range of the pulse height.

A typical reversible binary switching between LR and HR states is shown in Fig. 4. The resistance was read at $+1 \, V$ after applying each high voltage pulse. In this experiment, reversible switching effect induced by $\pm 20 \, V$ voltage pulses was recorded 50 times. Dynamic change in device resistance was up to two orders of magnitude. Fluctuations of resistances of HR and LR states might be due to some IR states. In the 50 recorded switching cycles, however, HR and LR states for binary storage are obviously distinguished (Fig. 5).

Consequently, a high negative pulse should be applied in order to obtain the LR state, while a high positive pulse
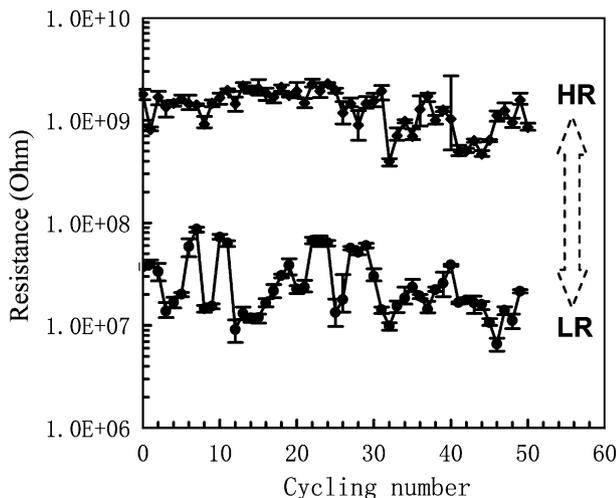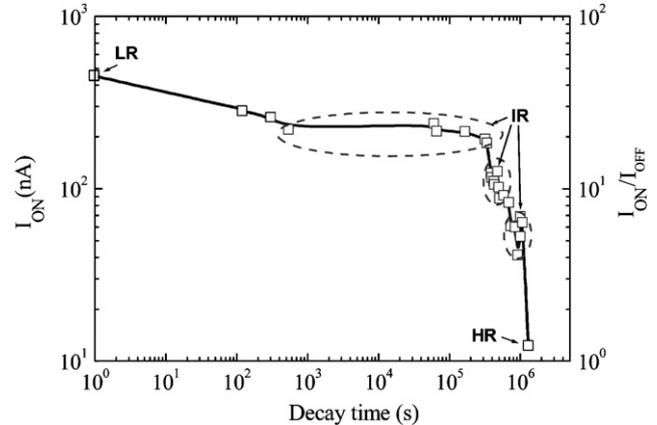
Fig. 5. Typical decay behavior of the device. Three IR states are relatively stable for a certain period.

should be applied to obtain the HR state here. A relatively high pulse is able to induce an IR state. READ operation can be performed by application of a small signal pulse.

3.3. Decay behavior via IR states

At first, the reversible switching of a device was performed for several cycles to ensure that the device worked well. I_{ON} and I_{OFF} currents of LR and HR states were measured at a low-voltage pulse of $+1 \, V$ after application of -20 and $+20 \, V$ pulses. I_{ON} and I_{OFF} of the device were 450 and $10 \, nA$, respectively. Then the I_{ON} current of the LR state after application of $-20 \, V$ voltage pulse was measured with time at $+1 \, V$. The ratio of I_{ON}/I_{OFF} reduced to unity about $1.5 \times 10^6 \, s$ after the pulse application. In other words, states of the MCM structures can be retained for about $1.5 \times 10^6 \, s$ (over 17 days) at room temperature if a binary storage is considered. We should also notice that there were three IR states when the LR state gradually decayed into the HR state. These IR states are relatively stable over time.

3.4. Discussion

Compared with PCM devices based on phase change, devices reported here exhibit the following special characteristics:

First, PCM devices are based on structural transformation, which depends strongly on input energy. Relatively high- and low-energy pulses usually are necessary to induce amorphization and crystallization of local region in chalcogenides, which were accompanied by the LR-to-HR and LR-to-HR changes in PCM devices, respectively. However, in our devices low and high power might be required for the LR-to-HR and HR-to-LR switchings. For instance, the LR-to-HR and HR-to-LR switchings according to switching points shown in Fig. 2 require approximately 50 and $150 \, \mu W$, respectively.

Second, switching of PCM devices depends on structural transformation and thus the crystalline LR state induced

Fig. 4. Typical reversible binary switching of the device. Resistance fluctuation of HR or LR states might be caused by some IR states.

by electrical pulses is very stable and retainable for a very long time such as 10 years at 120 °C for non-volatile memory [4]. However, the LR state here obviously decayed over time and the data can be retained for approximately 17 days at room temperature.

It is, therefore, very difficult to explain these unique characteristics exhibited by our devices in terms of structural transformation. Solid-state electrochemical reaction in the chalcogenide channel and formation and rupture of dendrite filaments across the channel [13–15] might be the reason for the bias polarity-dependent switching and IR states in the switching, as schematically illustrated in Fig. 6.

Ag or other neutral atoms indicated as M in Fig. 6 could become mobile cations after losing electrons when a negative voltage pulse is applied to the drain electrode based upon electrochemical reaction as shown in Fig. 6(a). These mobile cations migrate toward the negative electrode and filaments of dendrite of low resistivity form across the channel after the combination of cations and electrons. An LR state could consequently be obtained after the dendrite filament forms. On the contrary, confinement parts of the existing relatively small dendrites first break when a certain positive bias is applied to the drain electrode as shown in Fig. 6(b), by forming mobile cations and electrons. Some of dendrite filaments become discontinuous as illustrated in Fig. 6(b) by application of a bias relatively higher than threshold voltage V_{thl-h}, resulting in a relatively high-resistance state. Such a state might be one of IR states.
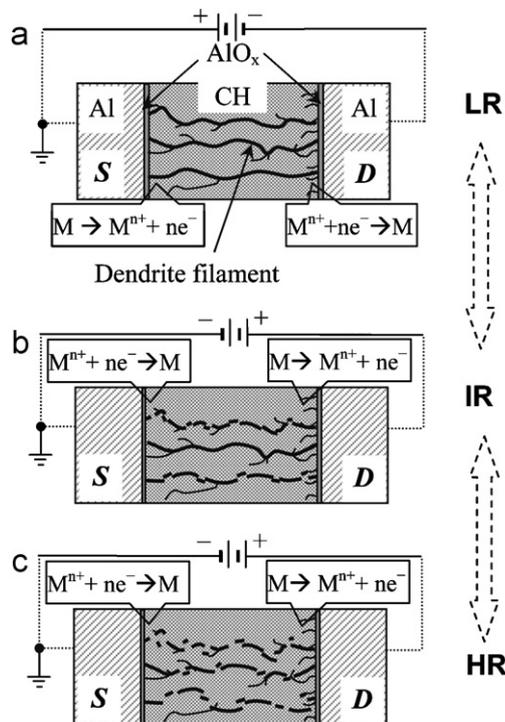
Finally, all of low resistive dendrites could break by a further increasing of pulse height, causing a HR state as illustrated in Fig. 6(c). As a result, polarity-dependent switching as shown in Figs. 2–4 might be attributed to the formation and rupture of dendrite filaments across the chalcogenide channel. The device resistance is related strongly to the number of dendrite filaments, which is controllable by electrical pulses. A series of resulting resistance states make multi-state storage feasible in the memory device.

The dendrite filaments induced by electrical pulses might not be sufficiently stable. Dendrite filaments form after a negative bias pulse is applied to the drain electrode, which results in a low-resistance state. However, atoms in dendrite might migrate and enter into vacancies [16] in the chalcogenides due to thermal fluctuations. The dendrite filaments would gradually become discontinuous over time. As a consequence, a LR state might finally decay into a HR state via some IR states as illustrated in Fig. 5.

The switching threshold voltage reported here was 10–15 V, but the corresponding currents shown in Fig. 2 are much lower than those of PCM devices. As is known, the RESET current for amorphization usually is higher than 1 mA at 180 nm technological node [4,5]. In this paper, the channel is as wide as 30 μm and gap is also as long as 3 μm. It is expected that the switching threshold voltage and current will scale with the gap length. We are investigating the dependence of switching voltage and current on the electrode width and gap length in order to further lower required power and switching voltage for practical application. Controllability of formation and rupture of filaments will be investigated for the study on multi-state storage in detail in the future.

4. Summary

A chalcogenide-based device with natural oxide on the electrodes exhibits some unique switching and memory behaviors compared with characteristics of reported PCM devices. I–V characteristics showed a reversible bias-polarity-dependent switching behavior via some intermediate states. Device resistance as a function of pulse height and decay behavior from a low-resistance state revealed that there were some intermediate states which were relatively stable in a certain voltage range and a certain period. These relatively stable intermediate resistance states make multi-state storage possible. These multi-states might be related to the number of dendrite filaments across the chalcogenide channel, which could be induced by electrical pulses.

Fig. 6. Schematic diagrams of the switching between (a) LR and (c) HR states via (b) IR states on the basis of solid-state electrochemical reaction and formation and rupture of dendrite filaments across the channel.

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